MODELS

PCI-IDO-48A,
PCI-IDO-32A,
and PCI-IDO-16A

Isolated FET Outputs PCI Card

With External Trigger Updates

USER MANUAL

Notice

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WARNING!!

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

Warranty

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

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If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

Coverage

First Three Years: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

Equipment Not Manufactured by ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

General

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

Table of Contents

Chapter 1: Introduction

The PCI-IDO-48A is a PCI board providing opto-isolated discrete outputs with load voltages up to 60VDC. Solid-state, P-Channel FET switches are used as the output elements providing greater reliability and much faster turn-on and turn-off time than is possible with electromechanical relays. Immediate and External Trigger modes offer flexibility for updating the outputs.

Features

- Up to 48 individually isolated digital Outputs
- Immediate and External Trigger Modes
- Trigger Over-run / Buffer Under-run error detection
- All solid-state design permits higher throughput than is possible with electromechanical relays
- Load voltages up to 60VDC
- Outputs off at power turn-on and computer reset
- Output connectors via on-card ribbon-cable headers
- Lower cost per point than externally-racked solid-state relay modules

Applications

- POS (Point-of-sale) Systems
- Gaming Machines
- Telecommunications
- Industrial Automation
- ATM (Automated Teller Machine) Systems
- Multiple terminal control
- Office Automation
- Kiosks

Functional Description

This series of cards provide 48, 32, or 16 opto-isolated discrete outputs. Each output is individually isolated using solid-state, P-Channel FET switches. These switches provide higher throughput in comparison to electromechanical relays. The outputs require user-supplied load voltages ranging from 5VDC to 60VDC. Diodes are included across the load for inductive-spike protection.

The outputs are grouped into six 8-bit bytes. There are two software selectable modes for updating the outputs: Immediate and External Trigger mode. Immediate mode updates the outputs as they are written. External Trigger mode stores the written output values into a buffer. The buffer contents are transferred to the outputs with a rising edge of the External Trigger. Outputs can be written multiple times without an External trigger occurring. However, only the last written values will be transferred upon a rising edge of the External Trigger. The Trigger Control Register can also be software configured to reset both the buffer contents and outputs on a falling edge. This allows pulse-width control of the outputs.

This board is also able to detect and count buffer underrun errors when using the External Trigger mode. A buffer underrun error occurs when a rising edge of the External Trigger happens before the outputs are written. Conversely, buffer overflow occurs when outputs are written more than once without an External Trigger rising edge. To prevent buffer overflow, a software readable bit can be polled to tell if a rising edge of the External Trigger has happened.

Refer to Chapter 5: Programming for details regarding the functions mentioned above.

Output connections are via three 50-pin IDC connectors, labeled Port0, Port1, and Port2 in this manual. Each Port contains sixteen outputs and Port0 also contains The External Trigger input.

Outputs are broken out using 50-wire ribbon cables that mate with the IDC connectors on the card. A strain relief bar where the cables exit the card assures that the cables will not interfere with adjacent cards. Standard cables are six feet long but alternate lengths are available.
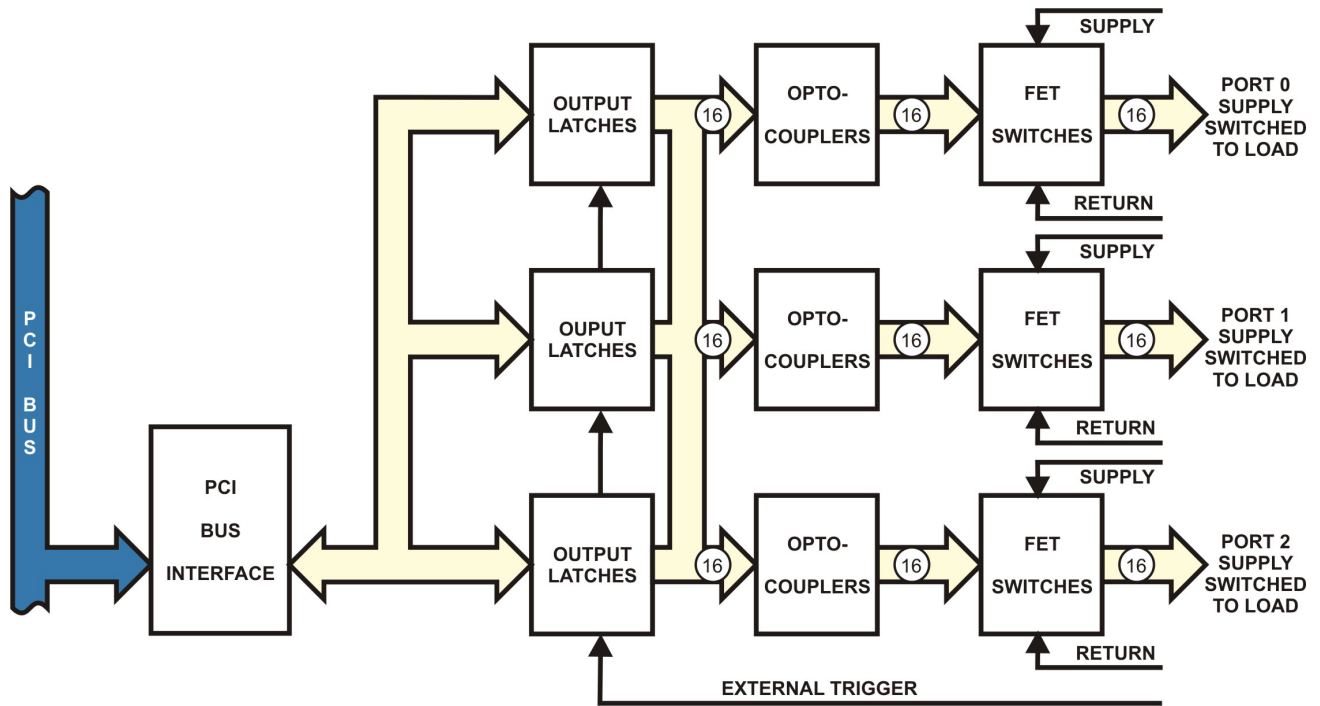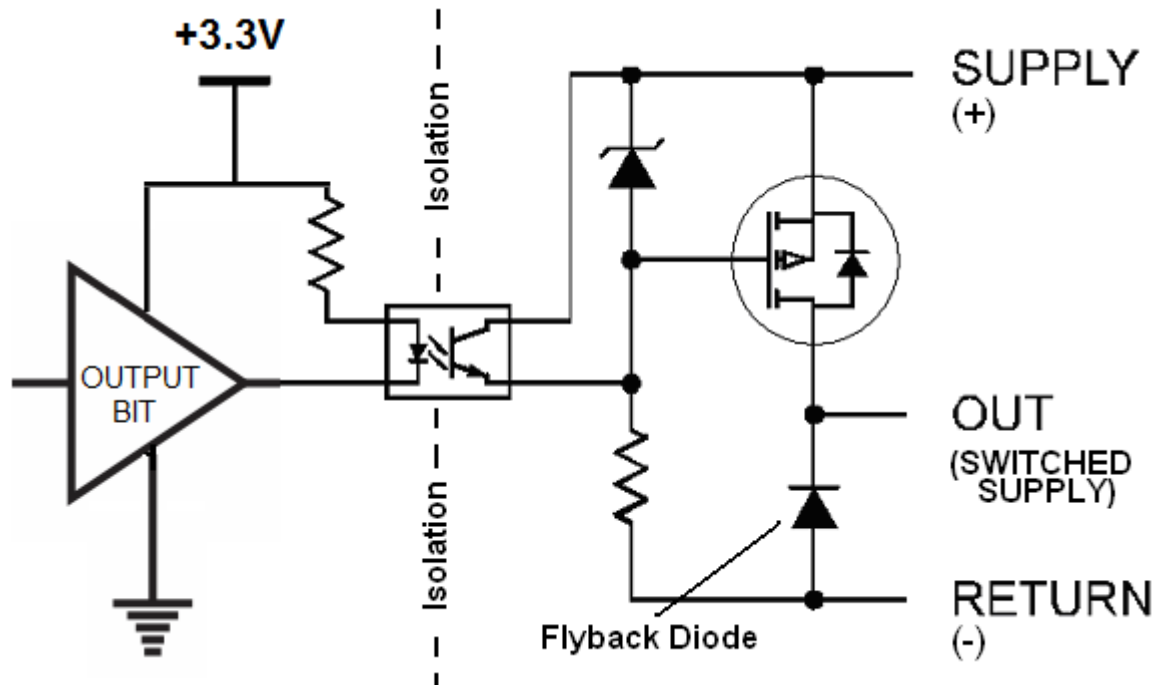

Figure 1-1: Block Diagram

Figure 1-2: Isolated FET Output Schematic

Note: FETs have two output states: Off, where the output is high impedance (no current flows between the VBB and the output — except for the FET's leakage current, amounting to a few µA), and On, where VBB is connected to the output pin.
Therefore, if no load is connected the FET output will have a high floating voltage (due to the leakage current and no path to the VBB switching voltages return). To mitigate this, please add a load to ground at the output.

Ordering Guide

- PCI-IDO-48A   48-Channel FET Output Board
- PCI-IDO-32A   32-Channel FET Output Board
- PCI-IDO-16A   16-Channel FET Output Board

Model Options

- -T   Extended temperature operation (-40° to +85°C)
- -RoHS   RoHS compliant version

Special Order

Please contact ACCES with your precise requirement. Examples of special orders would be conformal coating, custom software, etc., we will work with you to provide exactly what is required.

Included with your board

Manual PCI-IDO-48A Series

The following components are included with your shipment, <u>depending on options ordered</u>. Please take the time now to ensure that no items are damaged or missing.

- PCI FET Output Card
- Software Master CD
- Quick-Start Guide

Optional Accessories

• CAB50F-6	Six-foot ribbon cable assembly with 50-pin female connectors	
• STB-50	Screw terminal board, typically ships with standoffs but can also mount on SNAP-TRACK or DIN-SNAP	
• DIN-SNAP-6	Six inch length of SNAP-TRACK with two clips, for mounting one STB-50 screw terminal board on a DIN rail	
• STB-72CH	50-Pin Three-Header Universal Screw Terminal Board Installed in T-BOX Black Powder-Coated Metal Enclosure	
• MP104-DIN	Kit allows DIN rail mounting of STB-72CH in the T-BOX.	

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the card for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this card is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system.

CD Software Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.html on the CD-ROM for information on installing under linux.

Caution! * ESD   *A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.*

Hardware Installation

1.   Do not install card into the computer until the software has been fully installed.
2.   Turn OFF computer power AND unplug AC power from the system.
3.   Remove the computer cover.
4.   Remove the two (2) nuts retaining the strain relief brackets from the card, set one bracket aside with the nuts.
5.   Select an available location to install the card in an available 5V or 3.3V PCI expansion slot (you may need to remove a backplate first). DO not plug the card into the slot yet…..
6.   With the card in your hand or on the bench, feed ribbon cable(s) through the selected computer backplate one at a time and plug onto the card header, starting closest to the mounting bracket. When all cables are installed, re-install the strain relief bracket and nuts, and tighten until snug. DO NOT OVERTIGHTEN!
7.   Carefully plug the card into the slot and inspect for proper seating and fit. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
8.   Make connections from installed ribbon cables to the field equipment / wiring.
9.   Check all connections and installations to ensure the system is ready to be turned on. **Do not turn on field power before turning on the computer as all outputs on the card will be ON.**
10.   Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
11.   Run PCIfind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
12.   Run one of the provided sample programs that was copied to the newly created card directory (from the CD) to test and validate your installation.
13.   Once the card has been initialized and you're sure the outputs are in a known state, external / field power may now be turned on if desired.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck PCIFind or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In DOS, the PCI\SOURCE directory shows the BIOS calls used to determine the address and IRQ assigned to installed PCI devices. In Windows, the Windows sample programs demonstrate querying the registry entries (created by PCIFind and NTIOPCI.SYS during boot-up) to determine this same information.

Chapter 3: Option Selection
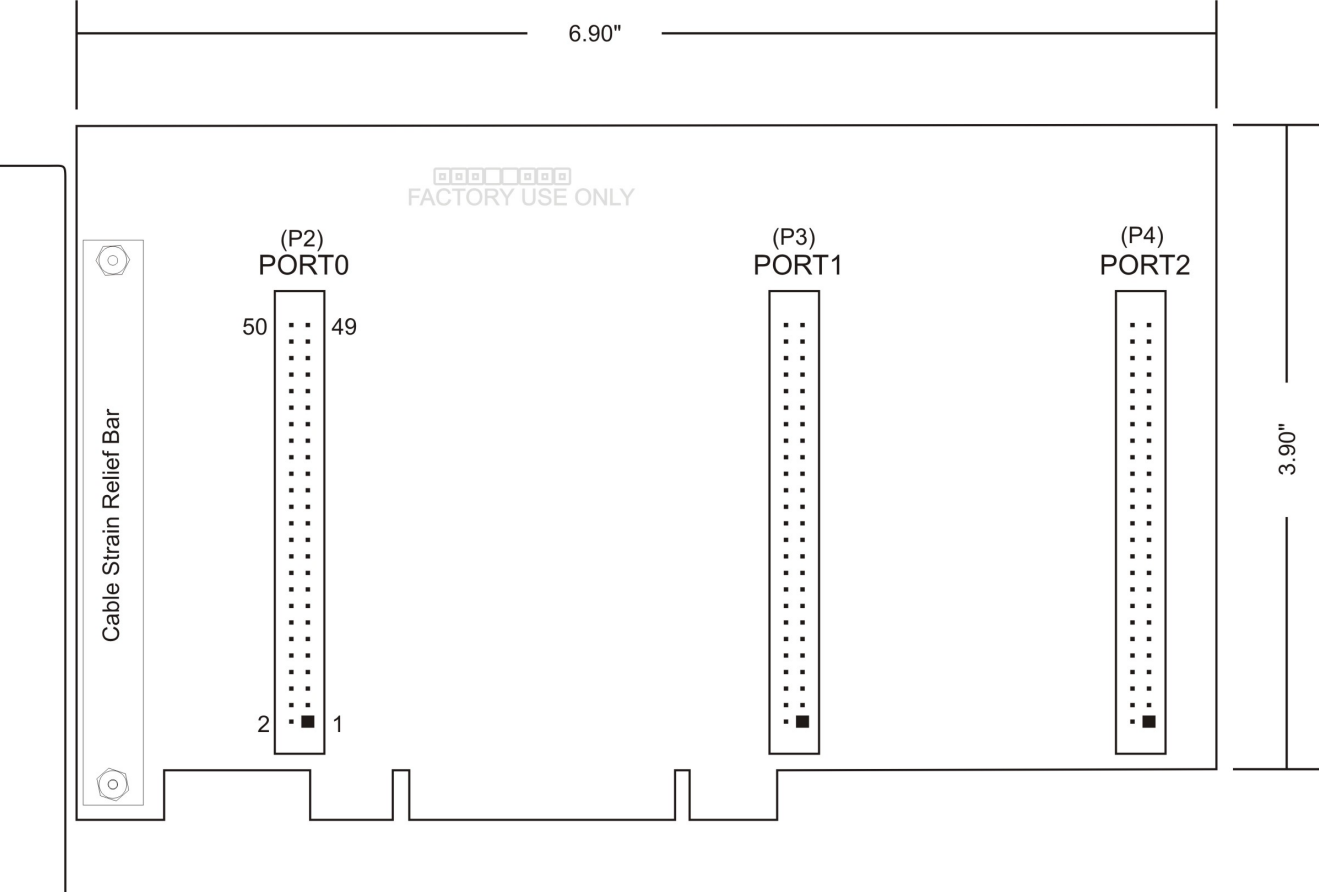
There are no user configurable options on this product.

Figure 3-1: Option Selection Map

Chapter 4: Address Selection

This card uses I/O addresses offset from the base address assigned by the PCIe bus. The address spaces are defined in the programming section of this manual.

PCIe architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCIe cards. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

The following information is for advanced users only:

The PCIe bus supports 64K of I/O address space, so your card's addresses may be located anywhere in the 0000h to FFFFh range.

To determine the base address that has been assigned, run the PCIFind utility program. This utility will display a list of all the cards detected on the PCI/PCIe bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, Windows systems can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind, or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

In Linux you can use the LSPCI command to determine this information. A PCIFind.pl script is also provided which may simplify this task.

An example of how to locate PCIe card resources in DOS is provided with in the PCI\SOURCE directory, under your installation directory. This code runs in DOS, and uses the PCI defined interrupt BIOS calls to query the PCI bus for card specific information. You will need the Device ID and Vendor ID listed above to use this code.

The card uses more resources than you usually need be concerned with. For clarity, PCIFind shows only the most commonly required information.

For those who require it, be aware of the following:
BAR[0]: memory mapped PEX8311
BAR[1]: I/O mapped PEX8311
BAR[2]: I/O mapped card registers (←all most software needs)

Chapter 5: Programming

The base address is assigned by the computer system during installation and will fall on an eight-byte boundary. The cards read and write functions are as follows:

Address	Write	Read
Base Address +0	Port 0 Bits 0-7	
Base Address +1	Port 0 Bits 8-15	
Base Address +2	Port 1 Bits 0-7	
Base Address +3	Trigger Control	Trigger Status
Base Address +4	Port 1 Bits 8-15	
Base Address +5	Port 2 Bits 0-7	
Base Address +6	Port 2 Bits 8-15	
Base Address +7		Trigger Over-run Count

Table 5-1: Register Address Map

Base Address + 0 (write) Port0 Low Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0

Writing to this address updates the data on Port0 bits 0-7. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

Base Address + 1 (write) Port0 High Byte

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
P0_15	P0_14	P0_13	P0_12	P0_11	P0_10	P0_9	P0_8

Writing to this address updates the data on Port0 bits 8-15. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

Base Address + 2 (write) Port1 Low Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0

Writing to this address updates the data on Port1 bits 0-7. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

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Base Address + 3 (read/write) Trigger Control/Status

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	trigEvent	trigReset	updateMode

The trigEvent bit is read only and is set to a '1' with a rising edge of the External Trigger. trigEvent is reset to a '0' on a read of Base Address + 3. The updateMode bit is read/write. Writing a '0' sets updateMode to External Trigger Mode and a '1' to Immediate Mode. The trigReset is read/write and only applies if updateMode is set to External Trigger Mode. Writing a '0' to trigReset will cause both the outputs and the output's buffer to be reset to zeros on a falling edge of the External Trigger. Writing a '1' causes the outputs and output's buffer to remain unchanged on a falling edge of the External Trigger.

Base Address + 4 (write) Port1 High Byte

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
P1_15	P1_14	P1_13	P1_12	P1_11	P1_10	P1_9	P1_8

Writing to this address updates the data on Port1 bits 8-15. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

Base Address + 5 (write) Port2 Low Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2_7	P2_6	P2_5	P2_4	P2_3	P2_2	P2_1	P2_0

Writing to this address updates the data on Port2 bits 0-7. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

Base Address + 6 (write) Port2 High Byte

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
P2_15	P2_14	P2_13	P2_12	P2_11	P2_10	P2_9	P2_8

Writing to this address updates the data on Port2 bits 8-15. The data is updated instantly to the outputs in Immediate Mode and updated on a rising edge of the External Trigger in External Trigger Mode. Refer to Base Address + 3 for Immediate and External Trigger Modes.

Base Address + 7 (read) Trigger Over-run Count

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Cnt3	Cnt2	Cnt1	Cnt0

Reading from this address will return the number of times (0-15) a rising edge of the External Trigger has occurred without writing to the outputs (Buffer Under-run Error).
The count value is reset to zero when read.

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Chapter 6: Connector Pin Assignments

Three identical 50-pin headers are provided on the product; one for each 16-bit output group. Port 0 (P2) is near the mounting bracket while Port 2 (P4) is at the far end of the card. Connector pin assignments are in the following three tables.

IDC 50-Pin Header Male

Pin	Signal	Pin	Signal
1	Ground / Trigger Return	2	Bit 0 Return (-)
3	Bit 0 Out	4	Bit 0 Supply (+)
5	Bit 1 Return (-)	6	Bit 1 Out
7	Bit 1 Supply (+)	8	Bit 2 Return (-)
9	Bit 2 Out	10	Bit 2 Supply (+)
11	Bit 3 Return (-)	12	Bit 3 Out
13	Bit 3 Supply (+)	14	Bit 4 Return (-)
15	Bit 4 Out	16	Bit 4 Supply (+)
17	Bit 5 Return (-)	18	Bit 5 Out
19	Bit 5 Supply (+)	20	Bit 6 Return (-)
21	Bit 6 Out	22	Bit 6 Supply (+)
23	Bit 7 Return (-)	24	Bit 7 Out
25	Bit 7 Supply (+)	26	Bit 8 Return (-)
27	Bit 8 Out	28	Bit 8 Supply (+)
29	Bit 9 Return (-)	30	Bit 9 Out
31	Bit 9 Supply (+)	32	Bit 10 Return (-)
33	Bit 10 Out	34	Bit 10 Supply (+)
35	Bit 11 Return (-)	36	Bit 11 Out
37	Bit 11 Supply (+)	38	Bit 12 Return (-)
39	Bit 12 Out	40	Bit 12 Supply (+)
41	Bit 13 Return (-)	42	Bit 13 Out
43	Bit 13 Supply (+)	44	Bit 14 Return (-)
45	Bit 14 Out	46	Bit 14 Supply (+)
47	Bit 15 Return (-)	48	Bit 15 Out
49	Bit 15 Supply (+)	50	Ext. Trigger Input

Table 6-1: Port 0 Connector Pin Assignments (P2)

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Pin	Signal	Pin	Signal
1	Ground	2	Bit 16 Return (-)
3	Bit 16 Out	4	Bit 16 Supply (+)
5	Bit 17 Return (-)	6	Bit 17 Out
7	Bit 17 Supply (+)	8	Bit 18 Return (-)
9	Bit 18 Out	10	Bit 18 Supply (+)
11	Bit 19 Return (-)	12	Bit 19 Out
13	Bit 19 Supply (+)	14	Bit 20 Return (-)
15	Bit 20 Out	16	Bit 20 Supply (+)
17	Bit 21 Return (-)	18	Bit 21 Out
19	Bit 21 Supply (+)	20	Bit 22 Return (-)
21	Bit 22 Out	22	Bit 22 Supply (+)
23	Bit 23 Return (-)	24	Bit 23 Out
25	Bit 23 Supply (+)	26	Bit 24 Return (-)
27	Bit 24 Out	28	Bit 24 Supply (+)
29	Bit 25 Return (-)	30	Bit 25 Out
31	Bit 25 Supply (+)	32	Bit 26 Return (-)
33	Bit 26 Out	34	Bit 26 Supply (+)
35	Bit 27 Return (-)	36	Bit 27 Out
37	Bit 27 Supply (+)	38	Bit 28 Return (-)
39	Bit 28 Out	40	Bit 28 Supply (+)
41	Bit 29 Return (-)	42	Bit 29 Out
43	Bit 29 Supply (+)	44	Bit 30 Return (-)
45	Bit 30 Out	46	Bit 30 Supply (+)
47	Bit 31 Return (-)	48	Bit 31 Out
49	Bit 31 Supply (+)	50	Ground

Table 6-2: Port 1 Connector Pin Assignments (P3)

Pin	Signal	Pin	Signal
1	Ground	2	Bit 32 Return (-)
3	Bit 32 Out	4	Bit 32 Supply (+)
5	Bit 33 Return (-)	6	Bit 33 Out
7	Bit 33 Supply (+)	8	Bit 34 Return (-)
9	Bit 34 Out	10	Bit 34 Supply (+)
11	Bit 35 Return (-)	12	Bit 35 Out
13	Bit 35 Supply (+)	14	Bit 36 Return (-)
15	Bit 36 Out	16	Bit 36 Supply (+)
17	Bit 37 Return (-)	18	Bit 37 Out
19	Bit 37 Supply (+)	20	Bit 38 Return (-)
21	Bit 38 Out	22	Bit 38 Supply (+)
23	Bit 39 Return (-)	24	Bit 39 Out
25	Bit 39 Supply (+)	26	Bit 40 Return (-)
27	Bit 40 Out	28	Bit 40 Supply (+)
29	Bit 41 Return (-)	30	Bit 41 Out
31	Bit 41 Supply (+)	32	Bit 42 Return (-)
33	Bit 42 Out	34	Bit 42 Supply (+)
35	Bit 43 Return (-)	36	Bit 43 Out
37	Bit 43 Supply (+)	38	Bit 44 Return (-)
39	Bit 44 Out	40	Bit 44 Supply (+)
41	Bit 45 Return (-)	42	Bit 45 Out
43	Bit 45 Supply (+)	44	Bit 46 Return (-)
45	Bit 46 Out	46	Bit 46 Supply (+)
47	Bit 47 Return (-)	48	Bit 47 Out
49	Bit 47 Supply (+)	50	Ground

Table 6-3: Port 2 Connector Pin Assignments (P4)

Chapter 7: Specifications

Outputs

Number of Channels:	48, 32, or 16
Load Voltage Range:	5VDC to 60VDC (Voltage supplied by User)
Load Current per Channel:	1A maximum steady state, 2A pulse (Note: Current may be limited by the cable. Certain ribbon cables limit current to 0.5A.)
Isolation:	On-Card Channel-to-channel and channel-to-computer (* see Note)
Switching Time:	Turn-On 50µs
	Turn-Off 5µs, inductive-spike protection via a diode
Switch Resistance:	0.4Ω when saturated
Switch Leakage Current:	25 to 250µA
Power Required	+5VDC @ 245mA (48 bits)

External Trigger Input

Type:	TTL; Pulled down to logic ground via 1k ohm resistor. Active update on rising edge (in reference to logic ground, requires a 2-wire connection, which is not isolated). Configurable to reset outputs on falling edge.
High:	2.0V min.
Low:	0.8V max.

*Note on Isolation: Opto-Isolators and connectors are rated for at least 500V, but isolation voltage breakdowns will vary and are affected by factors like cabling, spacing of pins, spacing between traces on the PCB, humidity, dust and other environmental factors. This is a safety issue so a careful approach is required. For CE certification, isolation was specified at 60V DC. The design intention was to eliminate the influence of common mode. Use proper wiring techniques to minimize voltage between channels and to ground. Tolerance of higher isolation voltage can be obtained on request by applying a conformal coating to the board.

Environmental

Operating Temperature:	0°C to +70°C
Storage Temperature:	-40°C to +150°C
Humidity:	5% to 90% RH, non-condensing
Board Dimensions:	6.875" (174.6mm) long, 4.2" (106.7mm) high

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: *manuals@accesio.com.* Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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